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EXAMINER	
WONG, BLANCHE	
ART UNIT	**PAPER NUMBER**
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/884,226	TRAVERSO ET AL.	
	Examiner	Art Unit	
	Blanche Wong	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-10,12-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5,8-10,12,14-18,20,21* is/are rejected.

7)☒ Claim(s) *4,6,7 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 2-10,12-18,20,21 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "phase equalizer" and "detector" (both in claim 12) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objections

4. Claims 9 and 21 are objected to because of the following informalities:

With regard to claim 9, Examiner suggests replacing "the predefined sequence" in line 5 with "pre-defined data sequence" in consistent with the claim language in claim 20.

With regard to claim 21, Examiner suggests replacing "is equal lot" in line 8 with "is equal to" to correct the typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. **Claims 2,3,5,8-10,12,14-18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 12, it is unclear what is meant by "appropriate" in line 3 where there are multiple selection signals and only one variable delay line. Additionally, as shown in Fig. 3, the variable delay elements, not the variable delay line, are driven by the respective selection signals.

With regard to claim 16, it is unclear whether the "enable signal generated by the detector" in lines 2-3 is the same as the "a detector ... generating an enable signal ..." in claim 21, line 4.

6. There is insufficient antecedent basis for this limitation in the claim.

Claim 2, line 3, "said input data flow".

Claim 3, lines 3-4, "the predefined data sequence containing a logic transition".

Claim 5, line 3, "the sampling operation".

Claim 8, line 2, "the result of said phase measurement operation".

Claim 10, line 2, "said input data flow".

Claim 14, line 2, "the phase equalizer".

Claim 17, line 3, "the sampled values".

Claim 17, line 3, "the selection signals".

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 2,12,18,20,21** are rejected under 35 U.S.C. 102(b) as being anticipated by Wiley (U.S. Pat No. 3,908,084).

With regard to claim 2, Wiley discloses a method of aligning data flows **(achieving phase synchronization, col. 1, line 67)** in time division frames **(time division, col. 3, line 52)** comprising the steps of:

measuring the phase **(frequency)** of an input data flow **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** with respect to the phase **(frequency)** of a reference signal **(clock signals on lead 27 in Fig. 3 at a frequency of 16 MHz, col. 4, lines 49-50)**, for controlling the delay time introduced by a delay line **(delay line 10 in Fig. 3, col. 4, line 55)** in said input data flow depending on the measured phase **(appropriate delayed phase)**, wherein the phase of the input data flow is measured in a time interval approximately corresponding to the transit time of a predefined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** comprised in said input data flow **(incoming pulses)**,

detecting **(detecting)** the flow of said predefined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** containing a logic transition **(logical zero, logical one) ("Arrival of a character start pulse is signified by a transition on the data channel from a steady-state logical zero conditions to a logical one pulse ...", col. 2, lines 36-38) (*See also* "The leading edge of the start pulse is the rightmost edge of the pulse", col. 5, lines 61-62)**, and

generating an enable signal **(a preferred one) ("a preferred one ... signals which are approximately centered, as a result of the consecutively delayed signals ...", col. 4, line s 60-62) (*See also* "the selected one", col. 5, line 11)** activating a phase sampling operation **(synchronized samples, col. 5, lines 9-10)**.

With regard to claim 12, Wiley discloses a phase alignment circuit **(selection circuit 12 in Fig. 3, col. 5, line 4)** of an input data flows **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** in time division frames **(time division, col. 3, line 52)**, comprising

a phase equalizer **(selection circuit)** for equalizing the phase **(frequency)** of a reference signal **(clock signals on lead 27 in Fig. 3 at a frequency of 16 MHz, col. 4, lines 49-50)** with the phase **(frequency)** of an input data flow **(incoming pulses)** and driving, through appropriate selection signals **(selecting the appropriate delayed phase) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**,

a variable **(nondelayed ... delayed ... fully delayed, col. 5, lines 48-49)** delay line **(selection circuit)** operating on the input data flow **(incoming pulses)**, wherein a detector **(selection circuit)** is provided for the transit **(arrival)** of a predefined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** containing a logic transition **(logical zero, logical one) ("Arrival of a character start pulse is signified by a transition on the data channel from a steady-state logical zero conditions to a logical one pulse ...", col. 2, lines 36-38) (*See also* "The leading edge of the start pulse is the rightmost edge of the pulse", col. 5, lines 61-62)** comprised in the input data flow **(incoming pulses)**, wherein said detector **(selection circuit)** controls the operation of the phase equalizer **(selection circuit)** through an enable signal **(a preferred one) ("a preferred one ... signals which are approximately centered, as a result of the consecutively delayed signals ...", col. 4, line s 60-62) (*See also* "the selected one", col. 5, line 11) (*See also* col. 5, lines 4-16)**.

With regard to claim 18, Wiley further discloses a ladder **(series arrangement, col. 5,line 49)** of delay elements **(*See also* 10-1,10-2 in delay line 10 in Fig. 4)**.

With regard to claim 20, Wiley discloses a method of aligning **(achieving phase synchronization, col. 1, line 67)** a data flow **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** in time division frames **(time division, col. 3, line 52)** comprising the steps of:

detecting **(detecting)** a pre-defined sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** contained in said data flow **(incoming pulses)**;

in response to detection of said pre-defined data sequence, generating an enable signal **(a preferred one)** during a time interval approximately **(approximately centered) ("a preferred one ... signals which are approximately centered, as a result of the consecutively delayed signals ...", col. 4, line s 60-62) (*See also* "the selected one", col. 5, line 11)** corresponding to a transit time **(arrival)** of said pre-defined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**;

in response to said enable signal, activating a measurement of the phase **(frequency)** of said data flow **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** with respect to the phase **(frequency)** of a reference clock signal **(clock signals on lead 27 in Fig. 3 at a frequency of 16 MHz, col. 4, lines 49-50)** in said time interval, wherein the frequency of said reference clock signal is equal to a nominal frequency of said data flow **(both frequencies are 16 MHz)**; and

controlling a delay time introduced by a delay line **(delay line 10 in Fig. 3, col. 4, line 55)** in said data flow depending on the measured phase **(appropriate delayed phase) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**.

With regard to claim 21, Wiley discloses a phase alignment circuit **(delay line 10 and selection circuit 12 in Fig. 3, col. 5, line 4)** of an input data flows **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** in time division frames **(time division, col. 3, line 52)**, comprising:

a detector **(selection circuit)** for detecting **(detecting)** a pre-defined sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** contained in said data flow **(incoming pulses)** and in response thereto generating an enable signal **(a preferred one)** during a time interval approximately **(approximately centered) ("a preferred one ... signals which are approximately centered, as a result of the consecutively delayed signals ...", col. 4, line s 60-62) (*See also* "the selected one", col. 5, line 11)** corresponding to a transit time **(arrival)** of said pre-defined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**;

a phase measurement circuit **(selection circuit)** responsive to said enable signal to measure the phase **(frequency)** of said data flow **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** relative to the phase **(frequency)** of a reference clock signal **(clock signals on lead 27 in Fig. 3 at a frequency of 16 MHz, col. 4, lines 49-50)** in said time interval, wherein the frequency of said reference clock signal is equal to the nominal frequency of said data flow **(both frequencies are 16 MHz)**; and

a time delay circuit **(delay line)** for controlling a time delay introduced by a delay line **(delay line)** in said data flow **(incoming pulses)** depending on the measured

phase **(appropriate delayed phase) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wiley in view of Lecourtier et al. (U.S. Pat No. 6,516,040).

With regard to claim 10, Wiley discloses a method of aligning data flows **(achieving phase synchronization, col. 1, line 67)** in time division frames **(time division, col. 3, line 52)** comprising the steps of

measuring the phase **(frequency)** of an input data flow **(incoming pulses arriving on data channel 8-1 in Fig. 3 at frequency of 16 MHz, col. 4, lines 46-49)** with respect to the phase **(frequency)** of a reference signal **(clock signals on lead 27 in Fig. 3 at a frequency of 16 MHz, col. 4, lines 49-50)**, and

controlling the delay time introduced by a delay line **(delay line 10 in Fig. 3, col. 4, line 55)** in said input data flow depending on the measured phase **(appropriate delayed phase) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)**, wherein

said measuring step comprises measuring the phase of the input data flow in a time interval **(appropriate delayed phase)** approximately corresponding to the transit time **(arrival)** of a predefined data sequence **(start pulse) ("...detecting an arrival of a character start pulse and selecting the appropriate delayed phase...", col. 5, lines 4-7)** containing a logic transition **(logical zero, logical one) ("Arrival of a character start pulse is signified by a transition on the data channel from a steady-state logical zero conditions to a logical one pulse ...", col. 2, lines 36-38) (*See also* "The leading edge of the start pulse is the rightmost edge of the pulse", col. 5, lines 61-62)**, said predefined data sequence **(start pulse)** being comprised in said input data flow **(incoming pulses)**.

However, Wiley fails to explicitly show a frame alignment word, and SDH or Sonet frames.

Lecourtier discloses a method of aligning data flows in time division frames wherein there are a frame alignment word **(start-of-frame patterns)** and SDH **(SDH) (SDH start-of-frame recognition patterns, col. 6, lines 37-38) (See also "... second remarkable property of the protocol SDH, which is that it has a means for identifying the start of a frame, ... 'start bit'", col. 6,lines 44-47)**.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine a frame alignment word and SDH as taught in Lecourtier with Wiley to provide for synchronization in high speed networking using SDH.

Allowable Subject Matter

11. Claims 4,6,7,13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 3,5,8,9,14-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blanche Wong whose telephone number is 571-272-3177. The examiner can normally be reached on Monday through Friday, 830am to 530pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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October 8, 2007

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